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Inventor(s): KNUDSEN DONALD CHRISTIAN ;

Applicant(s): KNUDSEN DONALD CHRISTIAN ;

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ABSTRACT:

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(71) Applicant  
**Donald Christian Knudsen**  
**R R #3, Perth, Ontario, Canada, K7H 3C5**

(72) Inventor  
**Donald Christian Knudsen**

(74) Agent and/or Address for Service  
**T Z Gold & Company**  
**9 Staple Inn, London, WC1V 7QH**

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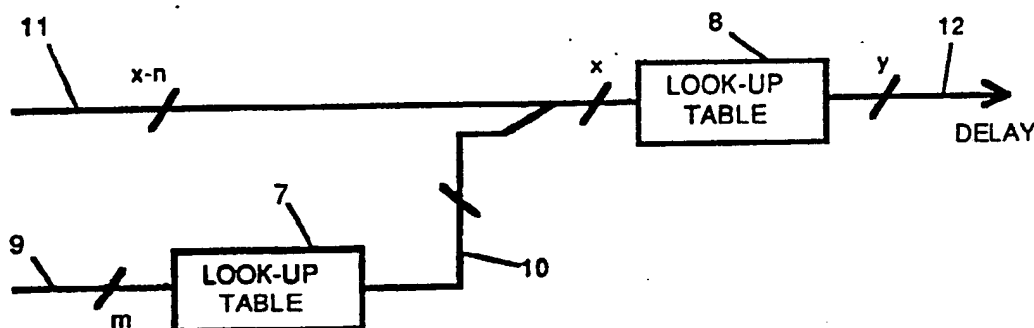
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**None**

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**G1G**  
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**G01S H01Q**

**(54) Digital delay generator for sonar and radar beam formers**

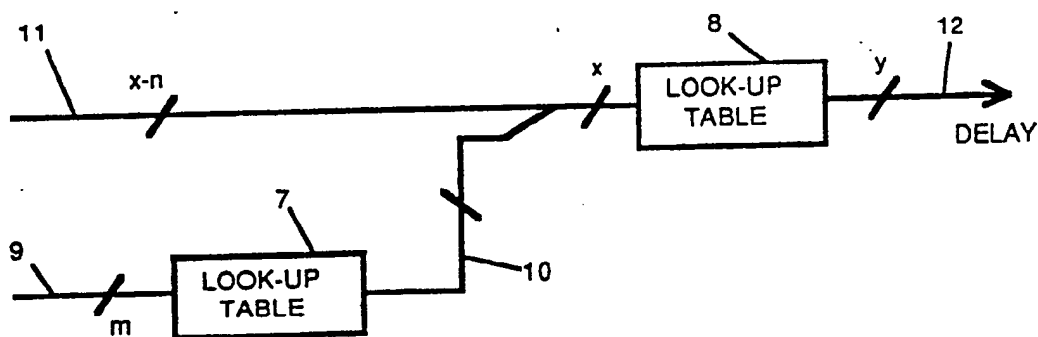
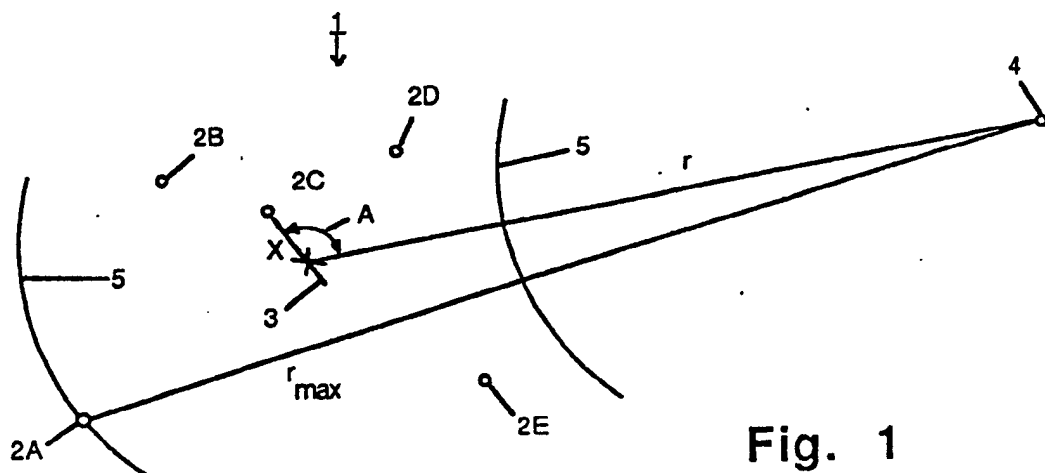
(57) Apparatus and a method of controlling the amount of delay or phase-shift which is applied to a signal received at or transmitted from each transducer in a multi-transducer antenna to produce a beam directed at a specific target point, includes, for each transducer, a first look-up table 7 for storing first digital words representative of the included angle between the lines joining the target to a reference point, and the same reference point to a transducer. A second look-up table 8 is associated with the first look-up table for each transducer, and stores second digital words representing delay or phase-shift control signals corresponding to ranges of the target relative to the reference point for each of said first digital words. Each first look-up table 7 is addressed with an address signal representing the direction of the line from the reference point to the target, to obtain a corresponding first digital word. Each second look-up table 8 is addressed with a corresponding first digital word combined with a signal representing the range of the target to obtain a corresponding second digital word. A signal received or transmitted by the corresponding transducer is delayed or phase-shifted an amount represented by the second digital word.



**Fig. 2**

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Fig. 3

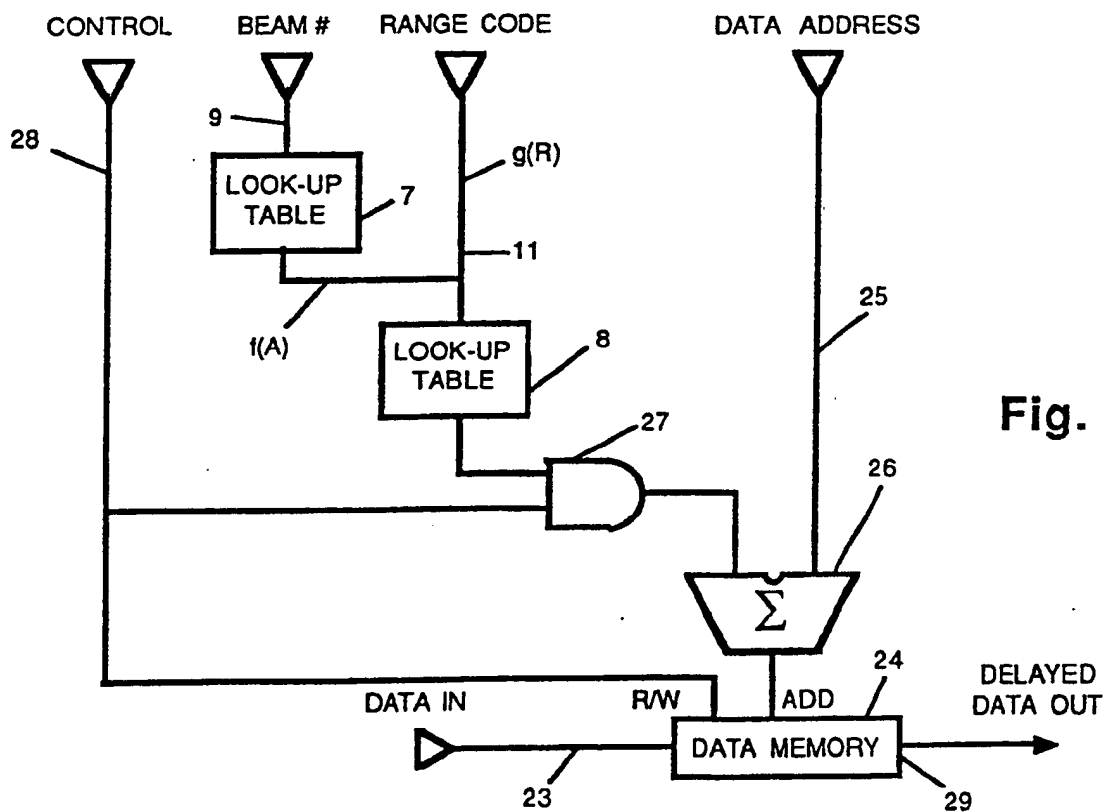
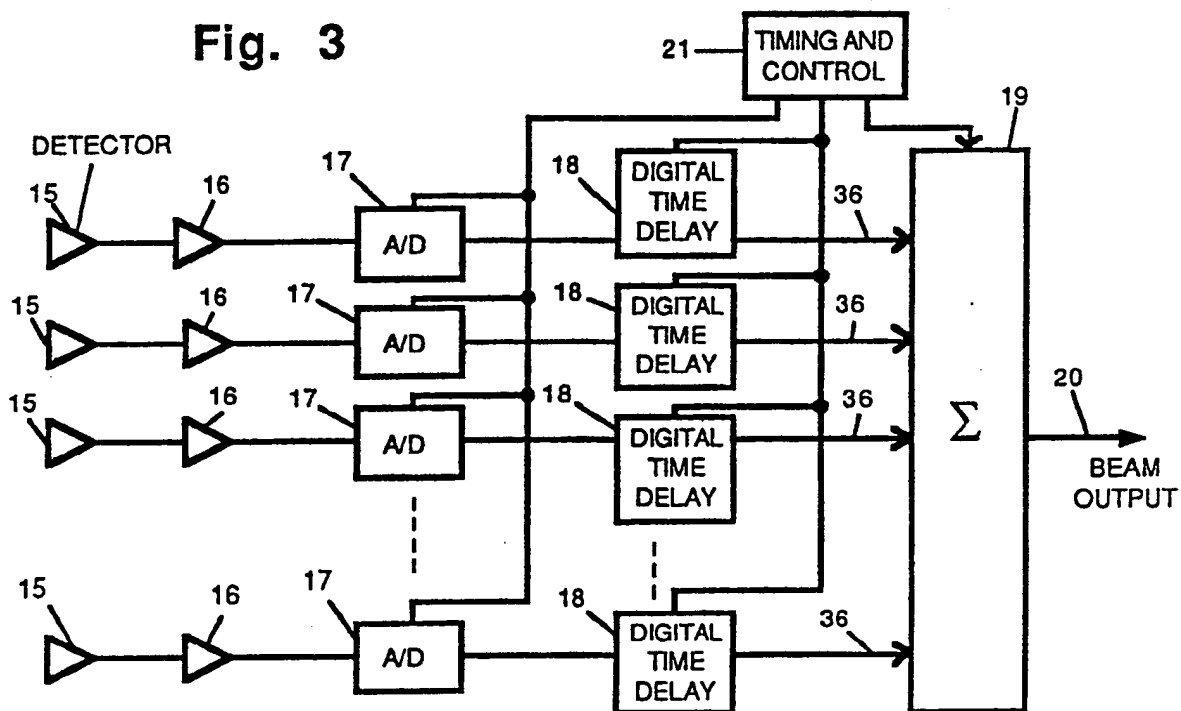


Fig. 4

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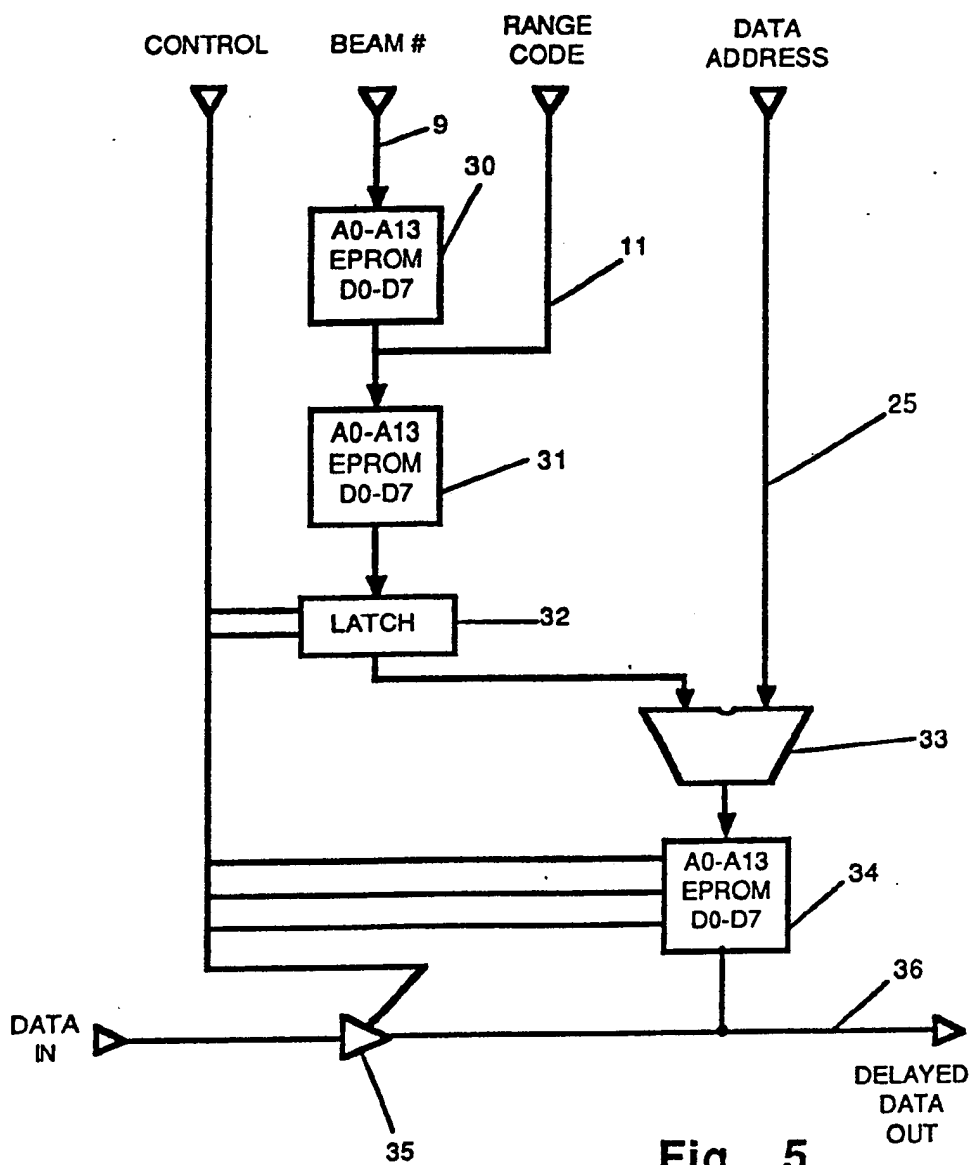


Fig. 5

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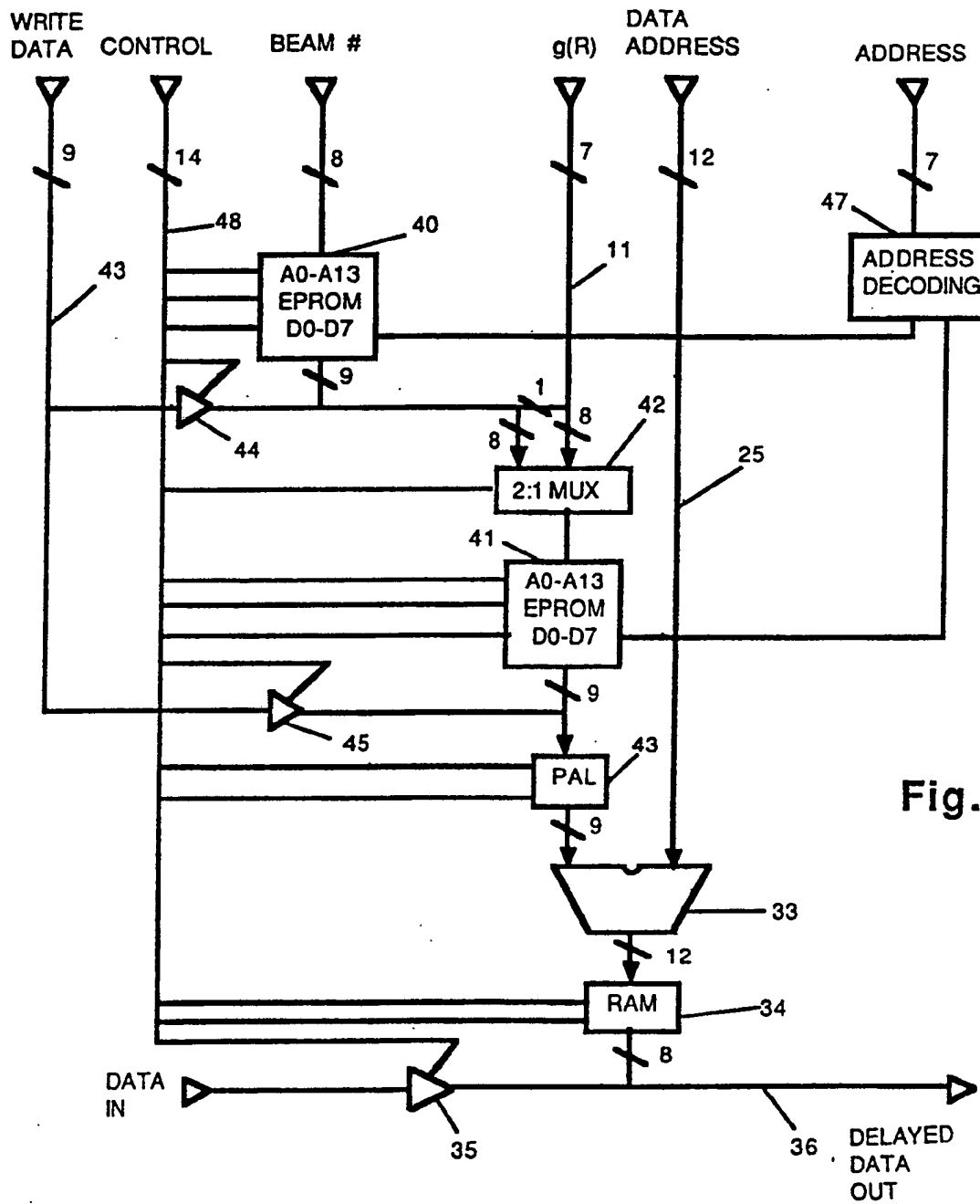


Fig. 6

DIGITAL DELAY GENERATOR FOR SONAR AND RADAR BEAM FORMERS

01  
02           This invention relates to electronically  
03 steered antennas such are used in sonar and radar  
04 systems, and particularly to an antenna beamformer for  
05 use in a multi-transducer array antenna.

06           A signal to be received from a specific  
07 source has a spherical wave front which is received by  
08 various transducers of a multi-transducer antenna at  
09 different instants in time. In order to correlate the  
10 signal wave front received by each transducer, the  
11 signals received by each transducer must be  
12 phase-shifted or time delayed. The delayed signals  
13 are then summed to form an output signal. The amount  
14 of time delay or phase shift introduced at each  
15 transducer is a parameter which is directly related to  
16 the radial distance from the specified source to the  
17 particular transducer. The antenna can be steered to  
18 any point in the object field by changing the delays  
19 which are applied to the signals at each transducer.

20           The implementation of a practical beam  
21 former using time delays of the signals received from  
22 each of the transducers and summing the result has  
23 proven to be a difficult problem. One of the major  
24 difficulties has been the lack of a satisfactory means  
25 for delaying the transducer signals individually by  
26 precise and controllable amounts. There are two  
27 aspects to this problem: the delay apparatus, and the  
28 delay control apparatus. This invention relates to  
29 the latter. The delay control apparatus is that part  
30 of a beam former which determines and controls the  
31 exact amount of delay which must be introduced at each  
32 transducer in order to steer the beam to a specified  
33 point in the object field.

34           A variety of electronic delay mechanisms  
35 have been tried or proposed, including analog delay  
36 lines, and charge coupled device analog shift  
37 registers. More recently, digital storage circuits  
38 such as semiconductor random access memories have been

01  
02 used as delay elements because of the large number of  
03 samples they can hold and the very fine delay  
04 resolution which can therefore be achieved.  
05 Regardless of the delay mechanism employed, however,  
06 the problem remains of determining the correct amount  
07 of delay to introduce in each case. The required  
08 delays are functions of the distances between each  
09 transducer and each point in the object field. In the  
10 general case of a three-dimensional transducer array  
11 with arbitrary, but known, transducer locations, and a  
12 three-dimensional object field, determination of the  
13 delay values involves a large number of moderately  
14 difficult computations.

15 This problem is usually minimised by  
16 restricting the array geometry in such a manner that  
17 symmetry and/or repetitiveness in the detector  
18 locations introduces a high degree of redundancy into  
19 the delay computations. The most obvious example of  
20 restricted geometry is the linear array with equally  
21 spaced elements. There are two significant  
22 disadvantages to restricting array geometry: the  
23 positions of the transducer elements must be a  
24 compromise between beam former design requirements and  
25 antenna performance considerations, and performance  
26 will inevitably suffer as a result, and the resulting  
27 beam former can only be used with arrays of the  
28 specific geometry for which the beam former was  
29 designed.

30 Another common method of increasing the  
31 degree of redundancy in the delay computations is to  
32 assume that all signals of interest originate  
33 sufficiently far from the detector array that their  
34 wave fronts are essentially planar across the aperture  
35 of the array. The disadvantage of this approach is  
36 that the antenna is incapable of focusing and is thus  
37 restricted to far-field targets. Although not a  
38 significant limitation for small aperture, low



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performance sonars, this inability to focus on near-field targets is unacceptable in large aperture, high resolution applications.

The redundancies introduced by the combination of restricted array geometry and the far-field approximation can reduce the quantity and complexity of delay computations considerably. For a few very simple array geometries, such as the linear array of equally spaced transducers, the computational requirements are negligible.

Another approach to the problem of delay value determination, which does not restrict array geometry or aperture, employs the general purpose digital computer. The detector signals are digitized and loaded into computer memory where the beam forming operation is performed entirely in software, usually in the frequency domain using Fourier transform techniques. Although offering unparalleled flexibility, this approach is unacceptably slow for many real time beam forming applications.

It is possible to pre-compute the delay values for each transducer for all possible points in the object field and store the results in look-up tables, one for each transducer, where they can be accessed very rapidly as required. This approach combines the flexibility of the general purpose computer with the speed of a dedicated hardware beam former, but it has the disadvantage that a three-dimensional object field with acceptable spatial resolution requires excessively large look-up tables. Thus for example to provide an acoustic imaging system with an object field of 128 pixels by 128 lines and the ability to focus at 64 different ranges, a look-up table for each transducer in such a system would have to contain 1,048,576 words. Clearly the memory requirements for such digital systems are extremely great.

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02           An example of a beam former using  
03 precomputed delay values stored in digital look-up  
04 tables is described by Petersen and Kino in "Real-time  
05 Digital Image Reconstruction: A Description of Imaging  
06 Hardware and an Analysis of Quantization Errors", IEEE  
07 Transactions on Sonics and Ultrasonics, Volume SV-31,  
08 Number 4, July, 1984, pp. 337-351. In this beam  
09 former the delay values are stored in a high-speed  
10 look-up table called a "focus map".

11           In these and all other known examples of  
12 beam former designs using pre-computed delay values  
13 stored in digital look-up tables, the array geometry  
14 is restricted in order to take advantage of symmetry  
15 and repetitiveness. The redundancy thus introduced  
16 into the delay computations reduces the size of the  
17 look-up table to manageable proportions. No prior  
18 example is known of a beam former using stored,  
19 pre-computed delay values for a three-dimensional  
20 transducer array of arbitrary geometry, to image a  
21 high-resolution, three-dimensional object field.

22           The present invention is a beam former  
23 apparatus which uses precomputed beam steering  
24 information stored in digital look-up tables to  
25 control the time delays introduced at each transducer  
26 of three-dimensional transducer array with arbitrary  
27 but known geometry to image a three-dimensional object  
28 field with high spatial resolution, and high speed  
29 (operating in real time), yet using substantially  
30 reduced memory from that required in the aforementioned  
31 prior art approach. For the case of an image field of  
32 128 pixels by 128 lines, focusing at 64 different  
33 ranges, rather than more than 1,000,000 digital delay  
34 words previously required for each of the transducers,  
35 the present invention requires only two memories, each  
36 storing 16,384 words. This clearly represents a  
37 substantial memory reduction over the prior art  
38 system. In a system to be described below, it has

01  
02 been found that depending on the duty cycle (the  
03 number of read cycles for every write cycle) beam  
04 output rates as high as 10,000,000 per second can  
05 easily be obtained.

06 In the present invention the look-up  
07 operation is partitioned in such a way that the  
08 excessively large look-up table previously required  
09 for each transducer can be replaced with two very much  
10 smaller look-up tables in a cascade configuration,  
11 thus providing a substantial net reduction in the  
12 total amount of look-up table memory required for each  
13 transducer.

14 The partitioning scheme utilizes the  
15 principle that the location of any point in  
16 three-dimensional object space can be fully defined by  
17 two direction coordinates and one range coordinate.  
18 Specifically, each target point can be defined by its  
19 distance (the target range) from a predetermined  
20 reference point, and by the direction (two  
21 coordinates) of the line from the reference point to  
22 the target. However, it can be shown that the  
23 beamsteering delay required at a particular transducer  
24 is a function only of the target range and the angle  
25 between the lines joining the predetermined reference  
26 point to the particular transducer and to the target,  
27 and is independent of the actual target direction.  
28 Thus the two direction coordinates of each object  
29 point can be replaced with a single parameter (for  
30 each transducer): the angle between the lines joining  
31 the predetermined reference point to the particular  
32 transducer and to the target. This angle, which is in  
33 general unique to each transducer and each target  
34 point, is sufficient to specify the required delay for  
35 any given value of target range.

36 Thus in the present invention, the first  
37 look-up table for each transducer transforms the two  
38 target direction coordinates into a digital

01  
02 representation of the angle between the lines joining  
03 the predetermined reference point to the particular  
04 transducer and to the target, and the second look-up  
05 table for each transducer transforms the digital value  
06 produced by the first look-up table for the  
07 transducer, together with the target range, into a  
08 digital delay control signal.

09         The present invention is a beam former  
10 control apparatus for a multi-transducer array antenna  
11 comprising a delay circuit for generating a delay or  
12 phase shift control signal for the signal received  
13 from (or, reciprocally, transmitted to) each  
14 transducer. Each delay circuit is comprised of a pair  
15 of look-up tables, the first look-up table receiving  
16 one or a pair of signals which specifies the direction  
17 of the beam. The input signals are representative of  
18 an address in the look-up table. The word which is  
19 read from the address in the first look-up table is  
20 output to the second look-up table. That signal, in  
21 combination with a second input signal which is  
22 representative of the range of the target, forms an  
23 address to the second look-up table. A word stored at  
24 the address of the second look-up table is output  
25 therefrom, and represents a delay, i.e. constitutes a  
26 delay control signal for the associated transducer for  
27 delaying the received signal prior to being summed in  
28 a summer with the separately delayed signals of the  
29 other transducers. In the case of a transmitting  
30 antenna, it controls the delay of the signal prior to  
31 being applied to the corresponding transmitting  
32 transducer. More generally, in accordance with one  
33 embodiment of the invention, each delay circuit is  
34 comprised of a first digital apparatus for receiving  
35 one or a pair of signals representative of a target  
36 direction relative to a predetermined reference point,  
37 which provides in response thereto a first signal  
38 representing a function of an included angle between

01  
02 lines joining the reference point to the corresponding  
03 transducer and the reference point to the target, and  
04 second digital apparatus in circuit communication with  
05 the first digital apparatus for receiving the first  
06 signal and a second signal representative of the range  
07 of the target relative to the reference point, and for  
08 providing in response thereto an output signal  
09 corresponding to the control signal.

10 In accordance with another embodiment of  
11 the invention, a multi-transducer array antenna is  
12 comprised of a plurality of digital time delay  
13 apparatus, one corresponding to each transducer for  
14 delaying transmission of a signal traversing  
15 therethrough, and including a delay control input.  
16 Analog-to-digital converter apparatus is connected to  
17 each transducer for receiving an output signal  
18 therefrom, having an output connected to an input of a  
19 corresponding time delay apparatus. A summer has  
20 inputs connected to corresponding outputs of the time  
21 delay apparatus, for receiving variously delayed  
22 output signals of the transducers and for providing a  
23 beam output signal of the antenna. Control apparatus  
24 controls the time delay of each time delay apparatus.  
25 Each control apparatus is comprised of a first look-up  
26 table for receiving a signal representative of the  
27 direction of the line joining the target to a  
28 predetermined reference point as an address, and for  
29 outputting in response thereto a first signal, stored  
30 at the address, representative of an included angle  
31 between lines joining the corresponding transducer to  
32 the reference point, and the reference point to the  
33 target of the corresponding transducer. A second  
34 look-up table receives the first signal and a second  
35 signal representative of the range of the target  
36 relative to the reference point as an address and  
37 outputs in response thereto a delay control signal  
38 stored at the address. The delay control signal is

01  
02 applied to a corresponding delay control input of a  
03 corresponding delay apparatus for controlling the  
04 delay of transmission of the signal from the  
05 corresponding transducer therethrough. Of course the  
06 look-up table can be combined into a single memory if  
07 the address requirements are dealt with in accordance  
08 with the art.

09 The signals representative of the  
10 direction and of the range of the target are provided  
11 from an external source which does not form part of  
12 this invention (e.g. from a manual control panel) and  
13 can simply be digitally converted signals  
14 corresponding to d.c. voltages established by a  
15 potentiometer connected across a d.c. power source, or  
16 equivalent apparatus. The transducers can be  
17 typically hydrophones in a sonar system, array  
18 elements of a radar antenna, etc.

19 A better understanding of the present  
20 invention will be obtained by reference to the  
21 detailed description below, in conjunction with the  
22 following drawings, in which:

23 Figure 1 is a schematic drawing  
24 illustrating the basic principles of a beam former,

25 Figure 2 is a block diagram illustrating  
26 the basic concepts of the present invention,

27 Figure 3 is a block diagram of a beam  
28 former which utilizes the present invention,

29 Figure 4 is a block schematic diagram of  
30 one embodiment of the invention which can be used in  
31 the configuration of Figure 3,

32 Figure 5 is a schematic of an embodiment  
33 of the invention, and

34 Figure 6 is a schematic of another  
35 embodiment of the invention.

36 Turning to Figure 1, the basic concept of  
37 the multi-transducer antenna beam former is  
38 illustrated. An antenna 1 is formed of representative

transducer 2A-2E which for purposes of illustration are arranged in a single plane. A reference point 3 and a target 4 are for illustration purposes located in the same plane as the transducers. The target 4 is a source of signals to be received (in the receiving case) which could be generating the signals or reflecting or scattering signals generated elsewhere. The speed of propagation in the medium is assumed to be the same at all points and in all directions, so the signals travel with spherical wavefronts from the target, as illustrated by line 5.

Clearly each wave front is interrupted by transducer 2E and 2D before being interrupted by transducer 2C which is earlier than the time that the same wave front is intercepted by transducers 2B and 2A. In order to correlate the signals from all transducers, the signals from transducers closer to the target must be delayed by amounts equal to the additional travel time that it takes the same wavefront to reach the transducer most distant from the target. The travel time from the target to any transducer is equal to the distance between the target and the transducer divided by the propagation speed in the medium. The required delays can therefore be expressed in terms of the array and object field geometry. With reference to Figure 1, the delay required at transducer 2C is defined by the expression:

$$\text{delay} = (r_{\max} - r) / c$$

where  $r_{\max}$  is a reference distance equal or greater than the distance between the target and the most distant transducer in the array,  $r$  is the distance between the target and transducer 2C, and  $c$  is the propagation speed of the received signal in the medium in which it travels,

The simplicity of this expression is deceptive, because in general  $r$  is not known explicitly, but must be computed or otherwise determined for each transducer from the known transducer and target coordinates every time a new target is selected. Furthermore, although the example was illustrated in two-dimensions, object fields are often three-dimensional, and may contain thousands of resolvable target points. The time required to perform these computations is particularly critical in real-time tracking, scanning and video applications which require the ability to change the steering delays very rapidly and frequently.

As was mentioned earlier, one way of achieving the above is to provide a transducer time delay control for each transducer comprising a memory which contains a look-up table for the time delay for each elemental position in three-dimensional object space for translation of the signal from each transducer. Thus for an object field of 128 pixels by 128 lines, and at 64 different ranges, the look-up table for each detector would have to contain 1,048,576 entries.

Instead, according to the present invention, a delay control apparatus is used for each detector as shown in Figure 2. In the present invention a pair of look-up tables 7 and 8 are used. An  $m$  bit address signal is applied to the  $m$  address lines 9 of look-up table 7, which address signal is representative of the beam direction for an associated transducer. A resultant output signal on the  $n$  output lines 10 of look-up table 7 is applied to  $n$  address input lines of look-up table 8. At the same time a range signal made up of  $x-n$  bits is applied to  $x-n$  address lines 11 which are input to look-up table 8. The resulting  $y$  bit output signal (with fewer number of bits than  $x$ ) from look-up table 8 on  $y$  lines 12



01  
02 represents the delay to be applied to the signal  
03 received from the associated detector array before  
04 summing with the signals from the other arrays (or  
05 alternatively applied to the signal to be transmitted  
06 from a corresponding transducer prior to being applied  
07 to that transducer).

08         The input signal on input lines 9  
09 represents beam direction. In the two-dimensional  
10 example of Figure 1, this direction could be specified  
11 by a single parameter, for example, the angle (from  
12 the horizontal) of the line between the target 4 and  
13 the reference point 3. In the general  
14 three-dimensional case two coordinates, azimuth and  
15 elevation for example, are required to unambiguously  
16 specify the beam direction.

17         In one example, the azimuth input signal  
18 to look-up table 7 could be formed of a 7 bit word.  
19 The corresponding elevation input would be similarly  
20 formed of a 7 bit word. Thus the address to look-up  
21 table 7 would be 14 bits. Yet the output word from  
22 look-up table 7 which is the function of the angle of  
23 A could be specified with e.g. 8 bits, an overall  
24 reduction of six bits or a factor of 64.

25         The output word is applied as part of an  
26 address signal to look-up table 8. The remainder of  
27 the address signal, representative of the range of the  
28 target is applied on input lines 11. The word  
29 representing the range would typically be 6 bits.  
30 Consequently the address of look-up table 8 would be  
31 14 bits.

32         The addressed delay control data stored in  
33 look-up table 8, is output on lines 12, would be e.g.  
34 8 bits, a substantial reduction from the input address  
35 word length. This output signal constitutes the delay  
36 control, with sufficient bit length to define the  
37 required resolution.

The look-up tables used in this example contain  $2^{14}$  (16,384) words each, for a total of 32,768 words, a substantial reduction from the 1,048,576 entries in the prior art approach.

The geometric basis for the present invention can be illustrated by rewriting the delay expression developed above in slightly different form. Referring again to Figure 1, the required delays can conveniently be specified relative to the time of arrival of the wave front at a real or hypothetical transducer located at the reference point 3. Recalling that the distance from the reference point 3 to the target 4 is defined as the target range, the amount of delay which must be applied to the signals from transducer 2C is equal to:

$$\text{delay} = d_{\text{ref}} + (R-r)/c$$

where  $d_{\text{ref}}$  is the delay required at reference point 3, and  
R is the target range.

The plane triangle formed by the target, the reference point and transducer 2C can be solved for r to permit the delay expression to be written as:

$$\text{delay} = d_{\text{ref}} + [R - (R^2 + x^2 - 2Rx \cos A)^{1/2}] / c$$

where A is the angle between the lines joining the reference point to the target point and to transducer 2C, and  
x is the distance between the transducer and the reference point.

Note that although illustrated in two-dimensions, this expression is fully valid in three-dimensional space.

The significance of this form of the delay expression is that, for any given transducer, the beamsteering delay is a function of only two variable parameters, R and A. Furthermore, the angle A is uniquely specified for any given transducer by the beam direction (the direction of the line from the reference point to the target point), and by the

01  
02 transducer location, and is independent of target  
03 range R. Thus, the two beam direction coordinates  
04 (e.g. pixel and line, or azimuth and elevation) can be  
05 transformed into a single intermediate parameter (A),  
06 quite independently of the range coordinate (R),  
07 thereby reducing the three-dimensional look-up  
08 operation to two, cascaded two-dimensional look-up  
09 operations. The delay signal has thus been  
10 transformed from a three-dimensional problem to a  
11 two-dimensional problem, requiring substantially  
12 reduced memory relative to a three-dimensional  
13 parameter storage memory.

14 Look-up tables 7 and 8 can be random  
15 access memories. A single chip 128k memory used for  
16 look-up table 7, for example type 27128, can  
17 accommodate a total of 16,384 distinct beam direction  
18 words. This is sufficient for an image field of 128  
19 pixels by 128 pixels or 360 increments in azimuth by  
20 45 in elevation. In the worst case (full spherical  
21 coverage) this size memory is capable of providing two  
22 degree resolution in both azimuth and elevation,  
23 although defining the beams in this manner may not be  
24 the most efficient use of look-up table addresses, if  
25 the criterion is uniform angular coverage of the  
26 object field. It should be noted that the address  
27 code can be regarded simply as a listing of the beam  
28 directions, in any convenient order (for example, a  
29 raster scan sequence), and the beams can be randomly  
30 accessed.

31 The address field of the 27128 memory chip  
32 is 14 bits wide. A similar memory chip can also be  
33 used for look-up table 8. Since 8 bits of the input  
34 address to look-up table 8 are used to specify the  
35 function of the angle A (the output from look-up table  
36 7) 6 bits are available for range data (x-n). The  
37 most efficient coding scheme is one which produces a  
38 uniform distribution of delay errors from infinity to

01  
02 the minimum distance at which the beam former can  
03 focus.

04 The effect of range resolution on the  
05 delay determination is highly non-linear, ranging from  
06 very large in the near field to insignificant in the  
07 far field. An unencoded range input would require a  
08 wastefully large look-up table address word length to  
09 provide acceptable resolution for near field target.  
10 For that reason it is desirable to increase the number  
11 of words stored for the near field ranges and decrease  
12 the number of ranges for the far field, i.e., inverse  
13 to the non-linearity.

14 Thus each time delay control circuit is  
15 identical, except for the data stored at each memory  
16 location of the look-up tables.

17 Figure 3 is a block diagram of a digital  
18 time delay and sum beam former. Transducers 15  
19 intercept the signals to be received from the target.  
20 The received signals pass through associated  
21 amplifiers 16 and the amplified signals are  
22 respectively applied to analog-to-digital converters  
23 17. Here the signals are converted to digital form,  
24 and are then applied to controllable time delay  
25 circuits 18. After being time delayed, the digitized  
26 signals from the transducers are applied to inputs of  
27 a summer 19, the output thereof being the beam output  
28 signal of the antenna, on transmission path 20. A  
29 timing and control circuit 21 controls the time delay  
30 in delay circuits 18, as well as the operation of  
31 analog-to-digital converter 17 and summer 19. The  
32 timing and control circuit 21 applies control signals  
33 to time delay circuits 18 to achieve electrical  
34 steering (beamforming) of the antenna to fulfill the  
35 delay characteristics required to identify the unique  
36 position in three dimensional space defined by the  
37 position of target 4 as described above with respect  
38 to Figure 1, within the resolution capability of the

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antenna.

Figure 4 illustrates the time delay circuitry, contained within each block of delay circuit 18 in Figure 3. Look-up table 7, receives a beam direction signal on input address lines 9. The address can be specified merely as a predefined beam number, which has been pre-standardized to represent a certain direction.

The output signal of look-up table 7 is applied via output lines 10, with a range address signal from input lines 11, to the address inputs of look-up table 8. The range input signal could alternatively be represented as a range code which has been predefined to represent a predetermined range. The range code and output signal of look-up table 7 together form an address input to look-up table 8, which in response outputs a delay control signal on output line 12.

The digitized signal received from the target via a transducer 15 is applied via input data line 23 to the data port DIN of a data memory 24. The write address to be added to the output data signal word from look-up table 8 is received on data address lines 25, which lines are connected to an input of a summer 26. The output signal of summer 26 is applied to the address input of data memory 24.

Preferably the data address source signals are generated in a counter which merely increments the address location for writing the input data from the transducer carried on data lines 23. Indeed, it is preferred that data memory 24 should be a rotating buffer which merely writes the data sequentially from one end of the memory to the other, starting again at the beginning, over-writing the old data once the end of the memory has been reached.

The delay signal from look-up table 8 is passed through AND gate 27, to the other input of

01  
02 summer 26. The second input of AND gate 27 is  
03 connected to a control input 28, which is also  
04 connected to the read-write R/W input of data memory  
05 24. The delayed input data is obtained at the data  
06 output line 29 from data memory 24. The delayed data  
07 output line 29 of each data memory is connected to a  
08 corresponding one of the inputs of summer 19 (Figure  
09 3).

10 In operation, external controller  
11 circuitry (not forming part of this invention)  
12 implements a write cycle. A write pulse is received  
13 at control line 28, connected to the R/W terminal of  
14 the data memory, and sets the data memory 24 to its  
15 write mode. At the same time AND gate 27 is  
16 inhibited. The data being received on input lines 23  
17 from an associated transducer is written to the data  
18 memory 24 at the address specified by the signals on  
19 data address source lines 25.

20 Assuming that data memory 24 has been  
21 filled with data from previous cycles, the data  
22 address increments, and the control input 28 switches  
23 to a read cycle. AND gate 27 is enabled, allowing the  
24 output data from look-up table 8 to pass through into  
25 summer 26. The address of the data on line 25 is thus  
26 incremented by the value of the output data from  
27 look-up table 8. The read address of data memory 24  
28 is thus an increment from that address which has just  
29 been written to, the increment representing a delay.

30 In this manner read and write cycles are  
31 time multiplexed; it is preferable that there should  
32 be several read cycles typically taking place for each  
33 write cycle. The beam output rate is thus made  
34 entirely independent of sample data input rate. The  
35 sample rate is determined by beam forming time-delay  
36 resolution requirements, rather than by sampling  
37 theory, and is normally much higher than the Nyquist  
38 rate.

01  
02           The time delay of a particular output  
03 sample is simply the difference between the read  
04 address and the write address multiplied by the  
05 sampling interval. It should be noted that it is the  
06 relative delay between the signals of the transducers,  
07 rather than the absolute amount of delay, that is  
08 important to beam forming.

09           The minimum capacity of the data memory,  
10 in terms of the number of samples it will hold, is  
11 determined by the sampling rate and the maximum delay  
12 required, which is a function of the ray geometry and  
13 steering angles. In practice a much larger data  
14 memory should be used so that several samples of each  
15 beam (in time sequence snap-shots) can be obtained  
16 without having to wait for new data.

17           The word size of the data memory can be as  
18 small as one bit, and in which case simple hard  
19 limiting circuits can be used instead of the  
20 analog-to-digital converters, or can be as large as  
21 desired. The choice of word size would normally  
22 depend on sonar or radar performance considerations  
23 rather than on beam former technology limitations.

24           It should also be noted that the beam  
25 number (direction) range code (range), the data  
26 address and the various control signals are generated  
27 externally and are common to all delay circuits in the  
28 system. The only difference between circuits  
29 associated with each transducer is the data stored in  
30 the look-up tables.

31           The adder 26 performs the functions of  
32 offsetting the delay relative to the current write  
33 address so that none of the delay values overlap the  
34 boundary between the old and the new data, and permits  
35 the controller to step through a time sequence of  
36 "snap-shots" of each beam.

37           Turning to Figure 5, an actual circuit  
38 implementation of the block diagram of Figure 4 is

shown. The eraseable programmable read-only-memories (EPROM) 30 and 31, each preferably type 27128 (128k) are used as look-up tables 7 and 8. The 14 address input ports A<sub>0</sub>-A<sub>13</sub> receive the beam number word or pair of words. The 8 data output ports D<sub>0</sub>-D<sub>7</sub> of EPROM 30 are connected to 8 address lines of EPROM 31, while 6 input lines which carry the range code are connected to the remaining address ports of EPROM 31, thus supplying a 14 bit address signal to ports A<sub>0</sub>-A<sub>13</sub>.

The 8 data output ports D<sub>0</sub>-D<sub>7</sub> of EPROM 31 (look-up table 8) are connected to the input of a type 273 latch 32. The output of latch 32 is connected to an input of a type 283 summer 33. Latch 32 performs the function of AND gate 27 (Fig. 4), and improves system speed by removing the look-up table access time from the data memory timing cycle. This is a benefit because the data memory would normally be accessed many times more frequently than the look-up table.

The data address signal (e.g. 11 bit) is applied to the other input port of summer 33 via lines 25, and the 11 bit output port of summer 33 is connected to the address ports A<sub>0</sub>-A<sub>10</sub> of data memory 34. Data memory 34 can be a 2k x 8 static random access memory (RAM).

The digitized input data from the transducer is passed through tri-state buffer 35, and is applied to the data ports D<sub>0</sub>-D<sub>7</sub> of data memory 34. The same port is used to read the delayed output data to output line 36.

The memories 30 and 31 could of course be larger, e.g. 512k to increase resolution, and as memory cost reduces, this would be desirable. Each memory as described is organized as 16,382 8 bit words, and thus memory 30 can accommodate a total of 16,384 distinct beam directions, which as noted earlier is sufficient for an image field of 128 pixels by 128 pixels, or 360 increments in azimuth by 45 in



elevation. Memory 31 produces an 8 bit delay value.

The remaining control lines for each of the memories (e.g.  $\overline{CS}$ ,  $\overline{WE}$ , etc.) are well known by persons skilled in the art and need not be described in detail.

Turning to Figure 6, another embodiment of the present invention is shown. In this embodiment, the look-up tables are implemented using dynamic random access memories (DRAMs) 40 and 41. Each memory has the capacity of 64k words by 9 bits per word. DRAM 40 is addressed similarly to memory 30 in the embodiment of Figure 5. However its data output lines  $D_0$ - $D_8$  are connected to one group of inputs of a 2:1 multiplexer 42 with the range code data, lines 11 being connected to the other group of inputs. The output port of multiplexer 42 is connected to the address inputs  $A_0$ - $A_7$  of DRAM 41. The data output lines  $D_0$ - $D_8$  of DRAM 41 are connected to the inputs of latch 43, and the outputs of latch 43 are connected to one set of inputs of adder 33. The other set of inputs of adder 33 is connected to the data address source lines 25, similar to the embodiment of Figure 5. The output of adder 33 is connected to the address inputs of random access memory 34 which, in this case, is a 4k word x 8 bit RAM.

The above-described circuit operates similarly as the circuit of Figure 5, except for the use of a multiplexer 42 for combining the output 9 bit signal of DRAM 40 and the 7 bit range signal together to form an 8 bit address word for DRAM 25. However the data stored in dynamic random access memories is volatile; the look-up table data must be downloaded from the system controller whenever the system is powered up. Being able to reload the look-up tables is very advantageous in applications in which the range geometry is slowly changing, such as when the

transducers are air-deployed drifting sonobuoys, e.g. used in military submarine locating systems. The use of 1-bit wide memories also permit greater flexibility in look-up table input and output word lengths, but at the expense of greater circuit complexity.

In order to load the memories, data to be written in them is provided on data lines 43 from the external controller. The data lines are connected to the data ports of memory 40 via tri-state buffers 44, and are connected to the data ports D<sub>0</sub>-D<sub>8</sub> of memory 41 via tri-state buffers 45. External control lines are connected to the control inputs of tri-state buffers 44 and 45 via bus 48.

Write address lines 46 carry memory selection signals for DRAMs 40 and 41 from an external controller to an address decoder 47 in which they are decoded. Output lines of decoder 47 are connected to the chip select inputs of random access memories 40 and 41.

To load the random access memories 40 and 41, the data is presented on the write data lines 43, and is passed through either one of tri-state buffer 44 or 45 under control of a buffer enable signal carried by the control bus 48. The memory selection address appears on address bus 46, which is decoded, and a resultant enable signal appears on the chip select input of memory 40. The data is loaded into the address defined by an address signal appearing on the input address lines 9.

The data to be loaded on the memory 41 is passed through the tri-state buffer 45 from the write data lines 43, memory 41 being enabled by a signal appearing on the address bus 46, which is decoded in address decoder 47, and applied to the chip select terminal of memory 41.

The look-up table data to be loaded appears at the data terminals D<sub>0</sub>-D<sub>8</sub> of memory 41 via

01  
02 buffer 45 and is loaded into the memory at addresses  
03 specified by address data which passes through  
04 tri-state buffer 44 under control of a signal on  
05 control bus 48 and address data applied to address  
06 lines 11. The address data passes through multiplexer  
07 42 to the address inputs A<sub>0</sub>-A<sub>7</sub> of memory 41. The  
08 address data passing through buffer 44 is of course  
09 not loaded into memory 40, since memory 40 at this  
10 time is inhibited by an inhibit signal appearing at  
11 its chip select input, as a result of the signal  
12 decoded from address bus 46 in decoder 47.

13 During normal non-loading operation of the  
14 circuit tri-state buffers 44 and 45 are placed in  
15 their non-conductive states by control signals on  
16 control bus 48. Both memories 40 and 41 are selected  
17 by means of an address signal appearing on an address  
18 bus 46, and decoded in decoder 47 to form the required  
19 chip select signals.

20 The beam direction selection signal is  
21 externally applied to address bus 9. The 9 bit word  
22 stored at the addressed location in memory 40 is  
23 output at the data outputs D<sub>0</sub>-D<sub>8</sub> of the memory, and  
24 appears at one of the input ports of multiplexer 42.  
25 At the same time, the 7 bit range signal is externally  
26 applied to lines 11, completing the address for memory  
27 41. Multiplexer 42 combines the two signals and  
28 applies an 8 bit address signal to the address ports  
29 of random access memory 41 which in turn outputs a 9  
30 bit delay signal stored at the address to latch 43.  
31 The 9 bit latched signal is applied to one of the  
32 ports of adder 33 which combines with the 12 bit data  
33 address signal on bus 25, and provides an address  
34 signal to random access transducer data memory 34.

35 An external controller can be designed by  
36 a person skilled in the art of controller design to  
37 provide the external signal requirements as described  
38 above. The remainder of the circuit operates

01  
02 similarly to that described above with respect to  
03 Figure 5.

04 The delayed transducer data output signal  
05 carried by lines 36 from each of the circuits  
06 described is applied to digital summer 19 (Figure 3)  
07 where it is added to provide the output signal of the  
08 antenna on transmission path 20.

09 The beam former described herein is  
10 inherently suited for expansion. This is accomplished  
11 very effectively by designing the basic beam former  
12 unit to accommodate a fixed number of transducer  
13 channels (64 for example), and expanding by operating  
14 two or more units in parallel.

15 Additional beam formers operating on the  
16 same transducer data in parallel can be used to  
17 increase the number of beam samples per second (of the  
18 same number of beams), or to increase the number of  
19 beams at the same beam output rate, or both. In  
20 either case a logical place to connect additional  
21 beam formers is following the analog-to-digital  
22 converters, to avoid functional duplication.

23 Similarly, two or more beam formers can be  
24 paralleled to handle a large number of transducers,  
25 although in this case the digital summer would have to  
26 be expanded.

27 The basic delay circuits described above  
28 are applicable to transmitting as well as receiving.  
29 In a transmitting application the transducer data  
30 memory (24 or 34) would be programmed with a suitable  
31 waveform (e.g. a chirp) and a digital-to-analog  
32 converter followed by a power amplifier would be  
33 connected to its output to drive an associated  
34 transducer element.

35 The beam former described above is  
36 applicable to either active or passive roles. When  
37 employed as a receive beam former in a sonar  
38 application, the range code generated by the system

01  
02 controller preferably is increased linearly with time  
03 following each transmit pulse so that the received  
04 echoes would always be in focus. In passive receiver  
05 applications the range function can be under operator  
06 control.

07           The design is also applicable to  
08 phase-shift beam formers. In fact, since fewer bits  
09 would normally be required to specify a phase shift  
10 than a time delay, the output word length of the  
11 second look-up table (reference 8 in Figure 4) could  
12 be reduced.

13           While the system embodiment described  
14 herein is directed to an acoustic sonar application,  
15 the system can also be used in radar systems as well,  
16 particularly phased array radar systems with a  
17 digitally controlled phase shifter. Low frequency  
18 radars such as those used for over-the-horizon  
19 applications could use the beam former directly in  
20 baseband.

21           The beam former described herein is also  
22 fully compatible with systems employing correlation  
23 processing of the beam signal output for pulse  
24 compression or for detection of coded pulses.

25           A person understanding this invention may  
26 now conceive of variations in design or other  
27 embodiments, using the principles described herein.  
28 All are considered to be within the sphere and scope  
29 of this invention as defined in the claims appended  
30 hereto.

CLAIMS

1. Beam former control apparatus for multi-transducer array antenna comprising:

a delay circuit for generating a delay or phase shift control signal for each transducer, each delay circuit comprising a first digital apparatus for receiving one or a pair of signals representative of a target direction relative to a predetermined reference point and for providing in response thereto a first signal representing a function of an included angle between lines joining the reference point to the corresponding transducer and the same reference point to the target, and a second digital apparatus in circuit communication with the first digital apparatus for receiving the first signal and a second signal representative of the range of the target relative to the reference point and for providing in response thereto an output signal corresponding to said control signal.

2. Apparatus as defined in claim 1 in which each of said digital apparatus is comprised of a first look-up table for receiving said representative target direction signals as a first look-up table address and in response for reading a corresponding digital word defining said first signal, and a second look-up table for receiving said first signal and said second signal as a second look-up table address and in response for reading a corresponding digital word defining said output signal.

3. Apparatus as defined in claim 1 or 2 in which the second look-up table contains more words

defining the near field delay values than far field delay values, whereby antenna resolution of the near field is rendered higher than that of the far field.

4. Apparatus as defined in claim 1 or 2 in which the look-up tables are comprised of random access memory means.

5. A multi-transducer array antenna comprising:

(a) a plurality of digital time delay means, one corresponding to each transducer, for delaying transmission of a signal therethrough, and including a delay control input,

(b) analog to digital converter connected to each transducer for receiving an output signal therefrom, having an output connected to an input of a corresponding time delay means,

(c) summing means having inputs connected to the outputs of the time delay means, for receiving output signals of the transducers and for providing a beam output signal of the antenna, and

(d) control apparatus for controlling the time delay of each time delay means, each control apparatus comprising a first look-up table for receiving a signal representative of the direction of a target relative to a predetermined reference point and for outputting in response thereto a first signal representative of an included angle between lines joining the reference point to a corresponding transducer and the same reference point to the target, and a second look-up table for receiving the first signal and a second signal representative of the range of the target relative to the reference point and for outputting in response thereto a delay control signal,

(e) means for applying the delay control signal to a corresponding delay control input of a

corresponding delay means for controlling the delay of transmission of a signal from a corresponding transducer therethrough.

6. An antenna as defined in claim 5 in which the look-up tables for each time delay means are comprised of random access digital memories storing words representative of said first signal and said delay control signals at predetermined address locations, said target direction signals being in the form of a beam direction specification constituting a first digital address for reading a word located at a corresponding address location, said second signal being in the form of a range code specification constituting a second digital address in combination with said first signal for reading a word located at a corresponding address location corresponding to said delay control signal.

7. An antenna as defined in claim 6 in which each time delay means is comprised of a digitally controlled phase-shifter.

8. An antenna as defined in claim 6 in which each time delay means is comprised of a data memory for writing digital signals output from a corresponding analog to digital converter, and for reading the data memory at an address specified by a corresponding delay control signal.

9. An antenna as defined in claim 8 in which the data memory is in the form of a rotating buffer, including means for writing said digital signals at sequential address locations, and means for reading said digital signals therefrom at sequential address locations spaced from writing addresses by an address increment defined by the delay control signal.



10. An antenna as defined in claim 9 including a latch connected to the data output of the second look-up table for temporarily storing the delay control signal for addressing the data memory.

11. A method of controlling the beam direction of a multi-transducer antenna comprising storing first digital words representative of included angles between lines joining a reference point to a transducer and the same reference point to the target, for each transducer in a corresponding look-up table, storing second digital words representing delay control signals corresponding to ranges of a target relative to the reference point for each of said first digital words in a second look-up table associated with the first look-up table for each transducer, addressing each first look-up table with an address signal representing the direction of said target to obtain a corresponding first digital word, addressing each second look-up table with a corresponding first digital word combined with a signal representing the range of the target to obtain a corresponding second digital word, and delaying a signal received by a corresponding transducer an amount represented by the second digital word.

12. A method as defined in claim 11 in which the number of bits in the first digital word is smaller than the number of bits in the address signal representing the direction of the target.

13. A method as defined in claim 11 or 12 including storing the signal received by each transducer at sequentially stored locations, and repeatedly reading the stored signal at locations offset from the storing locations by an amount represented by the second digital word.

28.

14. Apparatus according to claim 1 substantially as herein described with reference to and as shown in any of Figures 2 to 6 of the accompanying drawings.

15. An antenna according to claim 5 substantially as herein described with reference to and as shown in any of Figures 2 to 6 of the accompanying drawings.

16. A method according to claim 11 substantially as herein described with reference to and as shown in any of Figures 2 to 6 of the accompanying drawings.